Clocks

MM5316 digital alarm clock

general description

The MM5316 digital alarm clock is a monolithic MOS integrated circuit utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic required to build several types of clocks and timers. Four display modes (time, seconds, alarm and sleep) are provided to optimize circuit utility. The circuit interfaces directly with 7-segment fluorescent tubes, and requires only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, sleep (e.g., timed radio turn off), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The device operates over a power supply range of 8–29V and does not require a regulated supply. The MM5316 is packaged in a 40-lead dual-in-line package.

features

- 50 or 60 Hz operation
- Single power supply
- Low power dissipation (36 mW at 9V)
- 12 or 24-hour display format
- AM/PM outputs, Leading-zero blanking } 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Blanking/brightness control capability
- Elimination of illegal time display at turn on
- Direct interface to fluorescent tubes
- 9-minute snooze alarm
- Presettable 59-minute sleep timer

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block and connection diagrams

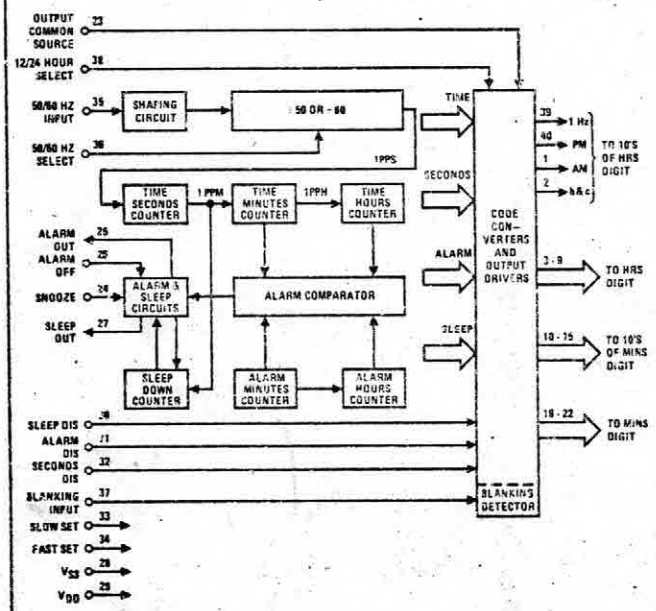
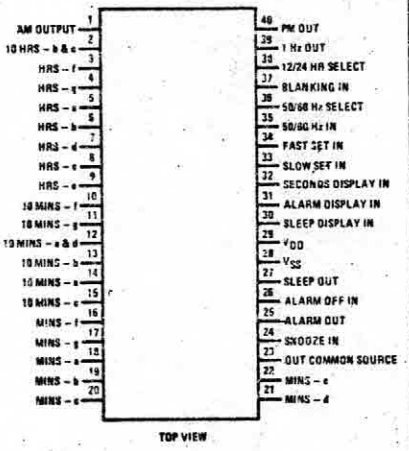


FIGURE 1.

Dual-In-Line Package



Order Number MM5316N
See Package 24

FIGURE 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 30V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 21V to +29V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	21		29	V
Power Supply Current	No Output Loads				
	V_{SS} = 8V			4	mA
	V_{SS} = 29V			5	mA
Counter Operation Voltage		8		29	V
50/60 Hz Input Frequency Voltage		dc	50 or 60	10k	Hz
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+1	V
Blanking Input Voltage					
Logical High Level		V_{SS}−1.5	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−4	V
All Other Input Voltages					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Device to V_{DD}	V_{DD}	V_{DD}	V_{DD}+2	V
Power Failure Detect Voltage	(V_{SS} Voltage)	10		20	V
Output Currents, 1 Hz Display	V_{SS} = 21V to 29V, Output Common = V_{SS}				
Logical High Level	V_{OH} = V_{SS} − 2V	1500			µA
Logical Low Level, Leakage	V_{OL} = V_{DD}			1	µA
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level	V_{OH} = V_{SS} − 2V	1000			µA
Logical Low Level, Leakage	V_{OL} = V_{DD}			1	µA
All Other Display, Alarm and Sleep Outputs					
Logical High Level	V_{OH} = V_{SS} − 2V	500			µA
Logical Low Level, Leakage	V_{OL} = V_{DD}			1	µA

functional description

A block diagram of the MM5316 digital alarm clock is shown in *Figure 1*. The various display modes provided by this clock are listed in Table I. The functions of the setting controls are listed in Table II. *Figure 2* is a connection diagram. The following discussions are based on *Figure 1*.

50 or 60 Hz Input (pin 35): A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt Trigger that is designed to provide about 6V of hysteresis. A simple RC filter, such as shown in *Figure 6*, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input (pin 36): A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving pin 36 unconnected; pull-down to V_{DD} is provided by an internal depletion device. Operation at 50 Hz is programmed by connecting pin 36 to V_{SS}.

Display Mode Select Inputs (pins 30–32): In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal pull-down depletion devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs (pins 33 and 34): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal pull-down depletion devices are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, in the 12-hour format (00:00:00 in the 24-hour format), by selecting seconds display and actuating both slow and fast set inputs.

Blanking Control Input (pin 37): Connecting this Schmitt Trigger input to V_{DD} places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display, (see *Figures 3 and 4*). Conversely, V_{SS} applied to this input enables the display.

Output Common Source Connection (pin 23): All display output drivers are open-drain devices with all sources common to pin 23 *(Figure 4)*. When using fluorescent tube displays, V_{SS} or a display brightness control voltage is permanently connected to this pin. Since the brightness of a fluorescent tube display is dependent on the anode (segment) voltage, applying a variable voltage to pin 23 results in a display brightness control. This control is shown in *Figure 6*.

12 or 24-Hour Select Input (pin 38): By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal depletion pull down device is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Segment connections for 10's of hours in 24-hour mode are shown in *Figure 5b*.

Power Fail Indication: If the power to the integrated circuit drops indicating a momentary ac power failure and possible loss of clock, the power fail latch is set. The power failure indication consists of a flashing of the AM or PM indicator at a 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. In the 24-hour format, the power failure indication consists of flashing segments "c" and "f" for times less than 10 hours, and of a flashing segment "c" for times equal to or greater than 10 hours but less than 20 hours; and a flashing segment "g" for times equal to or greater than 20 hours.

Alarm Operation and Output (pin 25): The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver *(Figure 4)*, the MM5316 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input (pin 24) or reset by the alarm "OFF" input (pin 26). If power fail occurs and power comes back up, the alarm output will be in high impedance state.

Snooze Alarm Input (pin 24): Momentarily connecting pin 24 to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm "OFF" Input (pin 26): Momentarily connecting pin 26 to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion device. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at V_{SS}.

Sleep Timer and Output (pin 27): The sleep output at pin 27 can be used to turn off a radio after a

functional description (Continued)

desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output via pin 27, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. The turn off may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the snooze input (pin 24). The output circuitry is the same as the other outputs *(Figure 4)*.

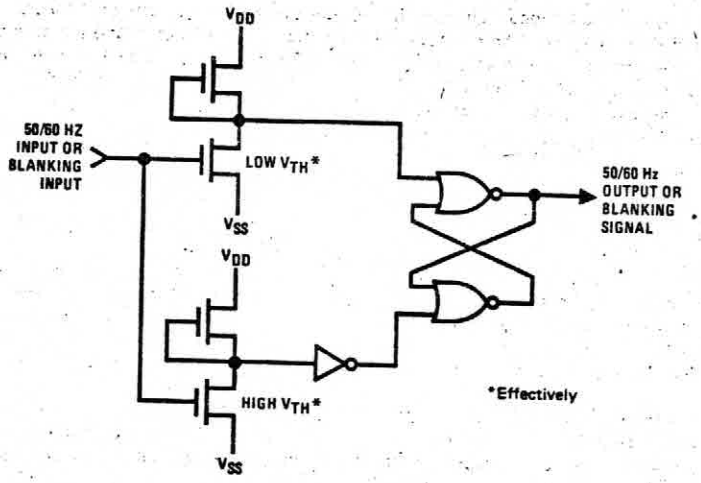
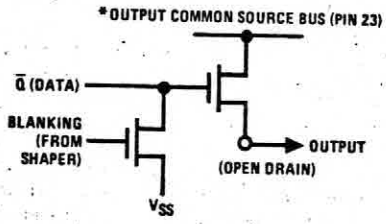
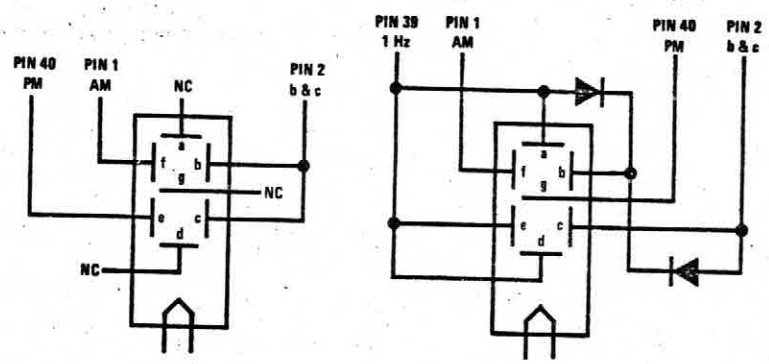


FIGURE 3. 50/60 Hz or Blanking Input Shaping Circuit



*Alarm and sleep output sources are connected to V_{SS}: blanking is not applied to these outputs.

FIGURE 4. Output Circuit



(a) 12-Hour Display Format (b) 24-Hour Display Format

FIGURE 5. Wiring Ten's-of-Hours Digit

functional description (Continued)

TABLE I. MM5316 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE II. MM5316 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 00:00:00 (24-hour format)
Sleep	Slow	Substracts Count at 2 Hz
	Fast	Substracts Count at 60 Hz
	Both	Substracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

typical application

Figure 6 is a schematic diagram of a general purpose alarm clock using the MM5316 and a fluorescent tube display.

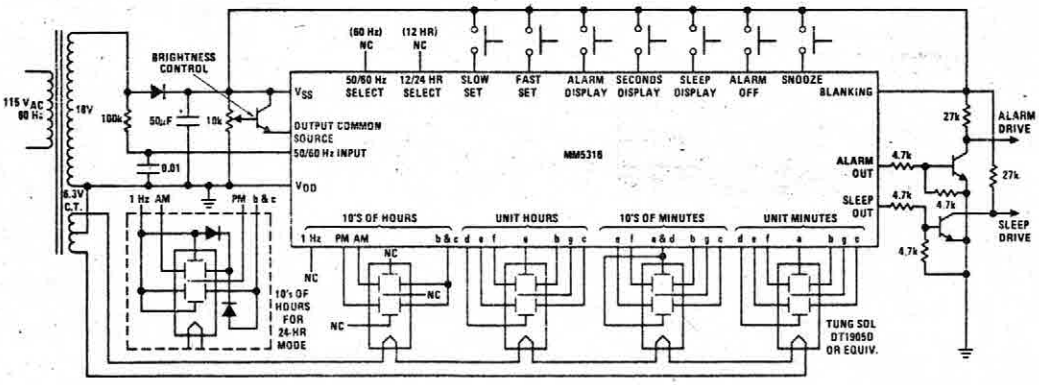


FIGURE 6. Schematic